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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/703,034	10/31/2000	Joseph R. Zbiciak	TI-30553	8913

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 10/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/703,034	ZBICIAK, JOSEPH R.	
	Examiner	Art Unit	
	Chat C. Do	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,5,9-11,13 and 16-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-5, 9-11, 13, 16-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 07/14/2004.

2. Claims 1, 4-5, 9-11, 13, and 16-24 are pending in this application. Claims 1, 13, and 18 are independent claims. In Amendment, claims 2-3, 6-8, 12, and 14-15 are cancelled and claims 18-24 are added. This action is made non-final.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 4-5, 10-11, 13, and 16-17 are rejected under 35 U.S.C. 103(a) as being obvious over Pitsianis et al. (Pub. No. US 2003/0088601 A1) in view of Adelman et al. (U.S. 5,666,300).

Re claim 1, Pitsianis et al. disclose in Figures 3B and 6 a method of performing a dot product operation with rounding and shifting in a microprocessor in response to a single rounding dot product instruction (Figure 3B with MPYCXD2 instruction), the method comprising the steps of: fetching a first pair of elements (Xr and Yi in 603 and 605) and a second pair of elements (Xi and Yr in 603 and 605); forming a first product (617) of the first pair of elements and a second product (619) of the second pair of elements; combining (625) the first product with the second product; form a combined product (output of 625) and rounding (627) the combined product to form an intermediate

result via an arithmetic circuit (627) having a first input receiving said first product, a second input receiving said second product and a carry input to a mid-position receiving said rounding value to form the intermediate result (Figure 2B with rounding architecture and col. 3 0049-0054 wherein the carry-input is a rounding factor according to conventional rounding architecture as ROUND, TRUNC, CEIL, or FLOOR and in Figure 3B the shifting/dividing is done prior rounding); and selecting the intermediate result a selected amount to form a final result (Ti in 629). Pitsianis et al. disclose a selector for selecting the higher bits, but Pitsianis et al. do not disclose the shifting the intermediate result. However, Adelman et a1. disclose in Figure 2 a shifter is placed at the end of operations to shift the operation result to certain amount prior storing the shifted results (54 into 6 1-62) due to limited bits storage. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to replace or add a shifter as seen in Adelman et al.'s invention into Pitsianis et al.'s invention because it would enable to improve the system performance for storing limited bits in register efficiently.

Re claim 4, Pitsianis et al. further disclose in Figures 3B and 6 the rounding value is 2^n and the selected shift amount is n+1 (col. 3 last 4 lines of 0054).

Re claim 5, Pitsianis et al. further disclose in Figures 3B and 6 n has a fixed value of fifteen (Figure 3B wherein 16-1 = 15).

Re claim 10, Pitsianis et al. further disclose in Figures 3B and 6-7 the step of combining comprises subtracting the product of second pair of elements from the product of first pair of elements (725 in Figure 7).

Re claim 11, Pitsianis et al. further disclose in Figures 3B and 6 the step of combining comprises adding the product of second pair of elements to the product of first pair of elements (625).

Re claim 13, it is a system claim of claim 1. Thus, claim 13 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 16, Pitsianis et al. further disclose in Figures 3B and 6 the step of shifting further includes sign extending the intermediate result (selecting only 30-15 out of 32 bits).

Re claim 17, Pitsianis et al. further disclose in Figures 3B and 6 the shifter right shifts the output of the arithmetic circuit the selected amount and sign extends the output of the arithmetic circuit (selecting only 30-15 out of 32 bits).

5. Claims 9 and 18-24 are rejected under 35 U.S.C. 103(a) as being obvious over Pitsianis et al. (Pub. No. US 2003/0088601 A1) in view of Adelman et al. (U.S. 5,666,300) as applied to claim 1 above, and further in view of Slavenburg et al. (U.S. 5,963,744).

Re claim 9, Pitsianis et al. in view of Adelman et al. do not disclose the steps of forming the first product and forming the second product treats a one of the first pair of elements as a signed number value and treats another one of the first pair of elements as an unsigned number value. However, Slavenburg et al. disclose in Figure 18 a dot product wherein the steps of forming the first product (e.g. first element of rsrc2 and rsrc1) and forming the second product (e.g. second element of rsrc2 and rsrc1) treats a one of the first pair of elements as a signed number value (rsrc2) and treats another one of

the first pair of elements as an unsigned number value (rsrc1). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the steps of forming the first product and forming the second product treats a one of the first pair of elements as a signed number value and treats another one of the first pair of elements as an unsigned number value as seen in Slavenburg et al.'s invention into the combined invention of Pitsianis et al. in view of Adelman et al. because it would enable to increase the flexibility of the system by handling multiple formatted operand registers (col. 2 lines 65-67).

Re claim 18, it is a similar method claim of claim 9 wherein the present claim has limitations cited in partially claim 1 and claim 9. Thus, claim 18 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claim 19, it is a similar method claim of claim 9 wherein the present claim further recited limitations in claim 1. Thus, claim 19 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claim 20, it has limitations cited in claim 4. Thus, claim 20 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 21, it has limitations cited in claim 5. Thus, claim 21 is also rejected under the same rationale as cited in the rejection of rejected claim 5.

Re claim 22, it has limitations cited in claim 16. Thus, claim 22 is also rejected under the same rationale as cited in the rejection of rejected claim 16.

Re claim 23, it has limitations cited in claim 10. Thus, claim 23 is also rejected under the same rationale as cited in the rejection of rejected claim 10.

Re claim 24, it has limitations cited in claim 11. Thus, claim 24 is also rejected under the same rationale as cited in the rejection of rejected claim 11.

Response to Arguments

6. Applicant's arguments with respect to claims 1, 4-5, 9-11, 13, and 16-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (703) 305-5655. The examiner can normally be reached on M => F from 7:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (703) 305-9662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2124

ANIL KHATRI
PRIMARY EXAMINER